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Self-Assembled Nanowires of Organic n-Type Semiconductor for Nonvolatile Transistor Memory Devices

*Ying-Hsuan Chou, Wen-Ya Lee, and Wen-Chang Chen**

Organic nonvolatile transistor-type memory (ONVM) devices are developed using self-assembled nanowires of n-type semiconductor, *N*,*N*′-bis(2-phenylethyl)-perylene-3,4:9,10-tetracarboxylic diimide (BPE-PTCDI). The effects of nanowire dimension and silane surface treatment on the memory characteristics are explored. The diameter of the nanowires is reduced by increasing the non-solvent methanol composition, which led to the enhanced crystallinity and high field-effect mobility. The BPE-PTCDI nanowires with small diameters induce high electrical fields and result in a large memory window (the shifting of the threshold voltage, ΔV_{th}). The ΔV_{th} value of BPE-PTCDI nanowire based ONVM device on the bare substrate can reach 51 V, which is significantly larger than that of thin film. The memory window is further enhanced to 78 V with the on/off ratio of 2.1×10^4 and the long retention time (10^4 s), using a hydrophobic surface (such as trichloro(phenyl)-silane-treated surface). The above results demonstrate that the n-type semiconducting nanowires have potential applications in high performance non-volatile transistor memory devices.

1. Introduction

Organic semiconductor have been widely studied for flexible electronic devices, such as light-emitting diodes,[1–4] photovoltaic cells,[5–11] field-effect transistors,[12–22] and nonvolatile memory[23–30] devices. Organic memory devices have attracted significant scientific interest owing to their advantages of the structural flexibility, processability, light weight, and 3D stacking capability.[31–35] Various device structures of resistor-, capacitor- and transistor-type memories, were proposed to fabricate organic memory devices with fast and reliability for data storage. Among them, organic field-effect transistor (OFET) memory devices showed the most noticeable characteristics owing to their easily integrated structure, non-destructive reading, and multi-bit storage in a single transistor.[35–37] The device configuration of OFET memory devices is the conventional transistors with an additional charge storage layer between a semiconductor layer and gate dielectric layer, such as ferroelectric materials,[37,38] metal nanoparticles,[16,39] or polymer electret layers.[40,41] The electrical switching of the OFET memory devices arose from charge trapped in chargeable polymer electrets[40,41] or polarization of ferroelectric materials.[37,38]

For complementary metal oxide semiconductor (CMOS) circuits with low-power dissipation and high operating speed, the developments of both p-type and n-type organic semiconductors are crucial. However, the progress of high mobility n-type organic semiconductors was behind that of p-type materials due to their low ambient stability. Recently, high-performance air-stable n-type semiconductors for OFET applications were developed, such as core-chlorinated naphthalene tetracarboxylic diimides,[42,43] dicyano-perylene-3,4:9,10-tetracarboxylic diimides (CN-PTCDI)[44] and poly(benzobisimidazobenzophenanthroline) (BBL).[45] However, relatively limited n-type organic semiconductors were explored for the applications of OFET memory devices. Facchetti et al. demonstrated a nonvolatile memory behaviors of n-type phenylene-thiophene oligomers with fluorinated groups, because long fluorinated groups could retain charges.[46] Organic semiconductors developed for OFET memory devices mainly focused on the p-type materials, such as pentacene,[36,47] poly(dioctylfluorene-co-bithiophene)[35,39] and phenylene-thiophene oligomers,[48] because the ambient oxygen and moisture could serve as electron traps significantly diminished the device performance in air,[49–55] restricting their memory device applications. Unlike p-type organic materials trapping electrons in dielectrics, the devices based on n-channel organic semiconductors enable reversible trapping of hole carriers in gate dielectrics. Therefore, the development of the n-type organic semiconductors for electrical memory applications may offer another direction toward high-performance nonvolatile memory devices.

Among n-type organic semiconductors reported in literature,[51,56–62] the PTCDI derivatives were extensively studied for one-dimensional organic nanowire electronics due to their high electron affinity and self-assembled nanostructures.[51,63] Through mixing good and poor solvents in an organic solution, so called solvent-exchange method, the PTCDI could self-assemble into a one-dimensional nanostructure via intermolecular π-π stacking.[64–69] Lambrecht et al.[70] prepared one-dimensional *N*,*N*-diperfluorophenyl-3,4,9,10-perylenetetracarboxylic diimide (DFPP) with a high aspect ratio and a moderate mobility of 10^{-3} to 10^{-4} cm^2 V^{-1} s^{-1}. Briseno et al. employed a solvent exchange method to prepare the complementary

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inverters based on n-channel PTCDI nanowire transistors and p-channel hexathiapentacene nanowire transistors.[71] Bao and coworkers developed an approach to align single crystalline nanowires of high charge transporting *N,N'*-bis(2-phenylethyl)-perylene-3,4:9,10-tetracarboxylic diimide (BPE-PTCDI).[33,34] However, n-type organic semiconducting nanowires for OFET memory applications have not been explored, as far as we know.

Herein, we report the nonvolatile transistor memory device characteristics of n-type organic semiconducting nanowires using BPE-PTCDI (**Figure 1**a). The diameters of BPE-PTCDI nanowires were controlled by the composition of the non-solvent (methanol) in the good solvent (*o*-dichlorobenzene), which led to different crystallinity. The effect of nanowire diameter on the charge storage capability of the BPE-PTCDI based top-contact OFET devices was investigated and compared to that of thin film. Furthermore, the surface modification using the self-assembly monolayers (SAMs) on the memory characteristics of BPE-PTCDI nanowires based devices were also explored, including trichloro(phenyl)silane (PTS) and trichloro(octyl)silane (OTS). To the best of our knowledge, this is the first report in the transistor-type memory devices using n-type organic semiconducting nanowires.

2. Results and Discussion

2.1. Optical Properties and Morphology

The self-assembled nanowires of BPE-PTCDI were formed through a solvent exchange processing from a concentrated good solvent (*o*-dichlorobenzene) into a non-solvent (methanol). The UV-vis absorption spectra of BPE-PTCDI in dilution solution, thin film and nanowires are shown in Figure 1b. The solution absorption spectrum of BPE-PTCDI shows the absorption bands at 535, 494, and 462 nm, attributed to the 0-0, 0-1, and 0-2 transitions of the vibronic structure of individual molecules, respectively.[71] The intensities of the vibronic transition bands are reduced with the increased composition of the non-solvent, suggesting that the BPE-PTCDI nanowires are appeared (see Figure S1 in the Supporting Information). The absorption peak maximum wavelengths (λ_{max}) of thin film and nanowire are observed at 617 and 652 nm, respectively, probably attributed to the π–π stacking of molecular self-assembly. The addition of methanol non-solvent could lead to the J-aggregates of the molecules and result in the large λ_{max} of BPE-PTCDI nanowires, similar to that reported in the literature.[64] The optical band gaps of BPE-PTCDI in solution state, thin films and nanowires estimated from the absorption edge are 2.25, 1.80, and 1.72 eV, respectively.

Through the solvent-exchange method, the diameters and the lengths of BPE-PTCDI nanowires were varied across a wide range. The dimensions of BPE-PTCDI nanowires were estimated from the SEM image (exampled by Figure 1c) and summarized in Figure 1d. The average diameter of BPE-PTCDI nanowires significantly decreases from 900 to 200 nm as the methanol non-solvent composition increases from 20 to 90 vol%, while the length reduces from 95 to 4 μm. When adding a large amount of the non-solvent, the BPE-PTCDI aggregates into nanowire immediately and thus leads to a small narrow size. The X-ray diffractograms (XRD) of the prepared BPE-PTCDI nanowires with different diameters are shown

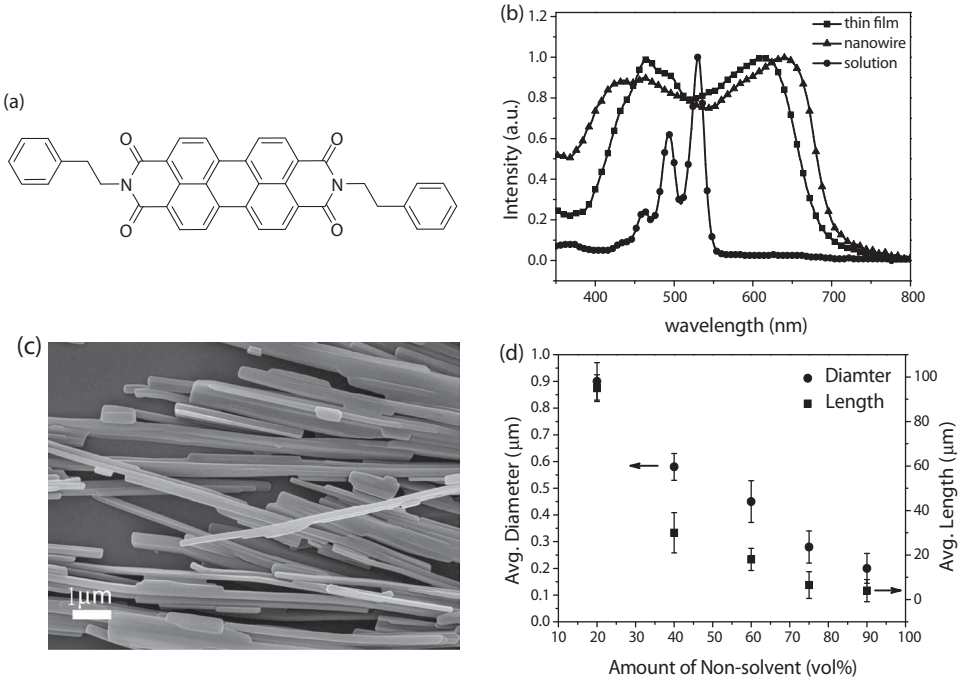

Figure 1. a) Chemical structure of BPE-PTCDI. b) UV-vis absorption spectra of BPE-PTCDI in the solution, thin-film, and nanowire. c) SEM image of the BPE-PTCDI nanowires induced by adding 60 vol% methanol non-solvent. d) Variation of average diameters and lengths of the BPE-PTCDI nanowires with non-solvent composition.

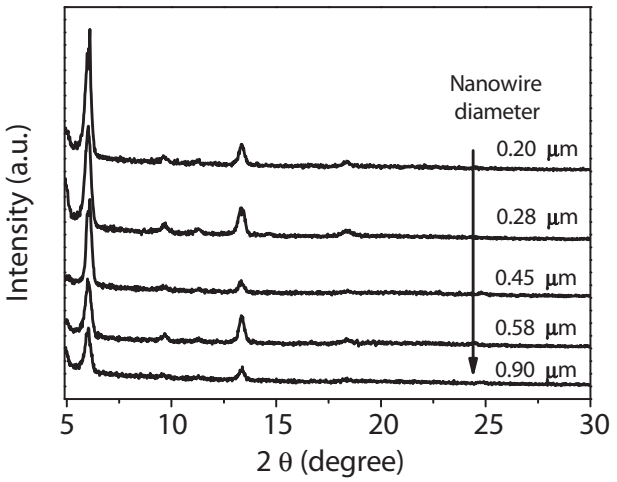

Figure 2. X-ray diffraction diagrams of the BPE-PTCDI nanowires with different diameters.

in **Figure 2**. All the nanowires show a well-defined diffraction (100) peak at 6.09°, corresponding d-spacing is 14.5 Å. Intriguingly, the peak intensity reduces gradually with increasing nanowire diameter. As discussed above, large nanowire diameter was obtained using a smaller quantity of non-solvent but this might cause more defects formed within the nanowires. In addition, the large amount of the non-solvent enhances the intermolecular interaction of BEP-PTCDI and thus leads to the high crystallinity, as evidenced in Figure 2. These results clearly reveal the quantity of the non-solvent significantly affect the dimension and the molecular packing of the BPE-PTCDI nanowires.

2.2. Effect of the Nanowire Diameter on OFET Memory Performance

Transistor-type memories based on these BPE-PTCDI nanowires were fabricated with a bottom-gate/top-contact configuration, as shown in **Figure 3**. Trichloro(phenyl)silane (PTS) and trichloro(octyl)silane (OTS) were used for the modification of the SiO_2 substrates. Note that the nanowires on PTS, OTS, and bare substrates are named as NW-P-1 ≈ 5, NW-O-1 ≈ 5, and NW-B-1 ≈ 5, respectively. **Figure 4** shows the typical output and transfer characteristics of BPE-PTCDI nanowire based OFET devices. As shown in the figure, the transfer curves of the NW-P-1 ≈ NW-P-5 nanowire devices exhibit good current

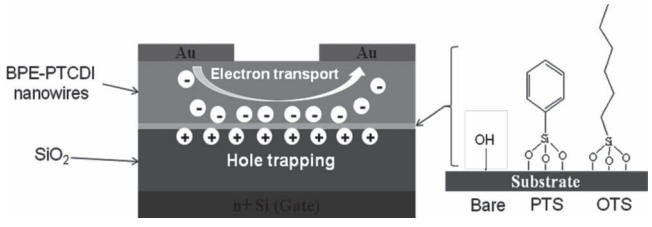

Figure 3. Schematic structure of the BPE-PTCDI nanowire based OFET memory device.

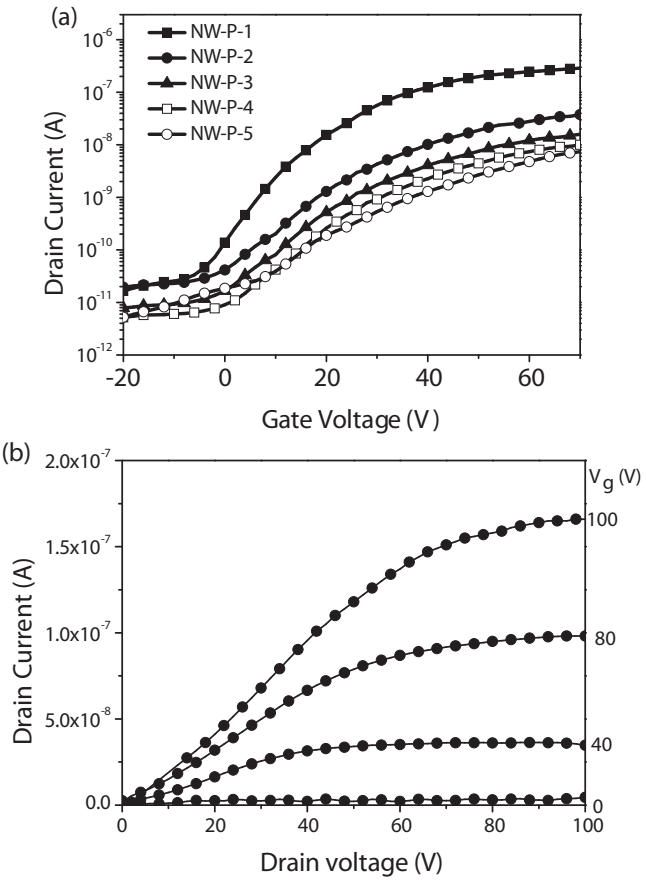

Figure 4. a) Transfer characteristics of the BPE-PTCDI nanowire (NW-P-1 ≈ NW-P-5) OFET devices on the PTS-treated substrate. b) Output characteristics of the NW-P-1 nanowire based OFET device.

modulation, and the output curves have well-defined linear and saturation regions. The sum of the width (W) and length (L) of the individual nanowires crossing the source and drain electrodes were used to estimate the active channel area for the calculation of charge mobility. The field-effect mobility was estimated from the plot of the square root of drain-to-source current $(I_{ds})^{1/2}$ versus the gate voltage (V_g) by the following equation in the saturation regime:[18]

$$I_{ds} = \frac{WC_i\mu}{2L}(V_g - V_{Th})^2 \quad (1)$$

where μ is the field-effect mobility; C_i is the gate dielectric capacitance per unit area; V_g is the gate voltages and V_{Th} denote the threshold voltages. V_{Th} was estimated from the x-axis intercept of the linear section of the plot of V_g vs $(I_{ds})^{1/2}$. The I–V_g characteristics of NW-P-1 ≈ NW-P-5 shown in Figure 4a indicate that the drain current enhances with decreasing the nanowire diameter. The OFET performance results of BPE-PTCDI nanowires are summarized in **Table 1**. The OFET mobilities of nanowires, NW-P-1, NW-P-2, NW-P-3, NW-P-4, and NW-P-5, on the PTS-treated substrates in the saturation region are 3.4×10^{-2}, 3.2×10^{-3}, 1.9×10^{-3}, 5.6×10^{-4}, and 4.9×10^{-4} $cm^2\ V^{-1}\ s^{-1}$, respectively. the V_{Th} values and the I_{on}/I_{off} current ratios range

Table 1. Characteristics of BPE-PTCI nanowire based OFET memory devices.

Sample	Substrate	Diameter (d) [μm]	Mobility [$cm^2 V^{-1} s^{-1}$]	V_{Th} [V]	On/Off [a]	Memory window [V][b]
NW-P-1	PTS	0.20	$(3.4 \pm 0.11) \times 10^{-2}$	(8 ± 1)	2.1×10^4	78
NW-P-2		0.28	$(3.2 \pm 0.14) \times 10^{-3}$	(10 ± 2)	2.8×10^3	62
NW-P-3		0.45	$(1.9 \pm 0.20) \times 10^{-3}$	(12 ± 1)	2.2×10^3	47
NW-P-4		0.58	$(5.6 \pm 0.37) \times 10^{-4}$	(13 ± 3)	3.6×10^2	37
NW-P-5		0.90	$(4.9 \pm 0.22) \times 10^{-4}$	(17 ± 2)	1.9×10^2	31
NW-O-1	OTS	0.20	$(4.3 \pm 0.21) \times 10^{-3}$	(9 ± 2)	3.8×10^3	54
NW-O-2		0.28	$(4.1 \pm 0.34) \times 10^{-3}$	(13 ± 3)	2.6×10^3	45
NW-O-3		0.45	$(3.1 \pm 0.58) \times 10^{-3}$	(15 ± 3)	1.1×10^3	36
NW-O-4		0.58	$(4.6 \pm 0.76) \times 10^{-4}$	(16 ± 1)	2.8×10^2	29
NW-O-5		0.90	$(1.1 \pm 0.69) \times 10^{-4}$	(17 ± 2)	1.5×10^2	26
NW-B-1	Bare	0.20	$(1.1 \pm 0.54) \times 10^{-3}$	(11 ± 3)	1.4×10^3	51
NW-B-2		0.28	$(3.2 \pm 0.66) \times 10^{-3}$	(14 ± 3)	7.8×10^2	40
NW-B-3		0.45	$(1.1 \pm 0.78) \times 10^{-4}$	(17 ± 1)	5.7×10^2	33
NW-B-4		0.58	$(8.7 \pm 1.02) \times 10^{-5}$	(18 ± 4)	2.3×10^2	22
NW-B-5		0.90	$(6.2 \pm 1.26) \times 10^{-5}$	(19 ± 4)	1.2×10^{-2}	20
Thin film	Bare[c]	-	$(1.8 \pm 0.39) \times 10^{-3}$	(2 ± 2)	–	5

[a] On/off drain current ratios of reading at $V_g = 0$ V; [b] ΔV_{Th} is defined as $V_{Th\ (erasing)} - V_{Th\ (writing)}$; [c] The performance of thin-film device on the bare substrate.

from 8 to 17 V and 10^3 to 10^5, respectively. The higher OFET mobility of the BPE-PTCDI nanowire with a smaller diameter is due to the larger crystallinity as evidenced in XRD.

To evaluate the electrical memory performance, the device was operated by applying appropriate gate pulse (±80 V) for one second to lead the shifts of the transfer curves. This thus resulted in the high- (ON state) and low-conductance (OFF state) states at zero gate bias conditions (V_g = 0 V). When applying a negative gate bias (V_g = –80 V for 1 s), the transfer curves were substantially shifted in the negative direction, served as the writing process, leading to a high drain current (ON state) at V_g = 0 V. When applied a reverse gate bias (V_g = 80 V for 1 s), the transfer curve shifted to positive direction served as the erasing process. Note that the shift range of the transfer curves through applying a writing and erasing gate bias is defined as the memory windows. **Figure 5** shows the transfer curves of the OFET memory devices based on the BPE-PTCDI nanowires and thin film. The nanowire device prepared on the PTS-treated (NW-P-1) and bare (NW-B-1) substrates show a large hysteresis with a memory window of up to 78 and 50 V, respectively. However, the thin-film device deposited on the bare substrate only exhibits a small memory window of 5 V. The larger V_{Th} shift of the nanowire device may be attributed to a higher electrical field generated in the confined dimension of the nanowires.[65]

The effect of nanowire diameter on the memory characteristics were investigated and summarized in Table 1 and Figure S5 (Supporting Information). The memory windows of NW-P-1, NW-P-2, NW-P-3, NW-P-4, and NW-P-5 OFET memory devices after applying a writing and erasing voltage are 78, 62, 47, 37, and 31 V, respectively. This indicates that the shifts on V_{Th} increases with the reduced diameter of nanowires, probably due to the enhanced electrical field of the smaller nanowires in the interface. The electric field of nanowires was shown to be much higher than that of thin film because the electric field was inverse proportional to the dimension.[72] The enhanced electrical field might facilitate the formation of dipole orientation at the dielectric-semiconductor interface, stabilizing charge trapping near the surface.[62] The trapped charges were released until the erasing voltage was applied. Katz and co-workers showed that the SiO_2 insulator in thin-film devices could be polarized when applying V_g = 100 V.[62] In the nanowire devices, the electrical field enhanced by the small diameter of the nanowires led to the stronger polarization of the SiO_2 dielectric compared to that of the thin-film devices. Therefore, the nanowire devices showed a large threshold-voltage shift. Moreover, the shifting on the threshold voltage (V_{Th}) of the nanowire based OFET memory devices enhanced with decreasing the nanowire diameters.

The shifts in memory window (ΔV_{Th}) can be used to estimate the amount of stored charges (Q) according to Equation (2):[39]

$$\Delta V_{Th} = -\frac{d_i Q}{\varepsilon_i} = -\frac{Q}{C_i} \quad (2)$$

where C_i is the dielectric capacitance of total dielectrics and ΔV_{Th} is the memory window. With a dielectric capacitance C_i = 10.9 nF cm^{-2}, the numbers of trapped charges are 5.31×10^{12}, 4.22×10^{12}, 3.20×10^{12}, 2.52×10^{12}, and 2.11×10^{12} cm^{-2} for NW-P-1, NW-P-2, NW-P-3, NW-P-4, and NW-P-5, respectively. This reveals that the smallest nanowire is capable of possessing the largest number of trapped charges.

2.3. Effects of the Self-Assembly Monolayer

The surface modification of self-assembly monolayers (SAMs) on the dielectric layer had a significant influence on the

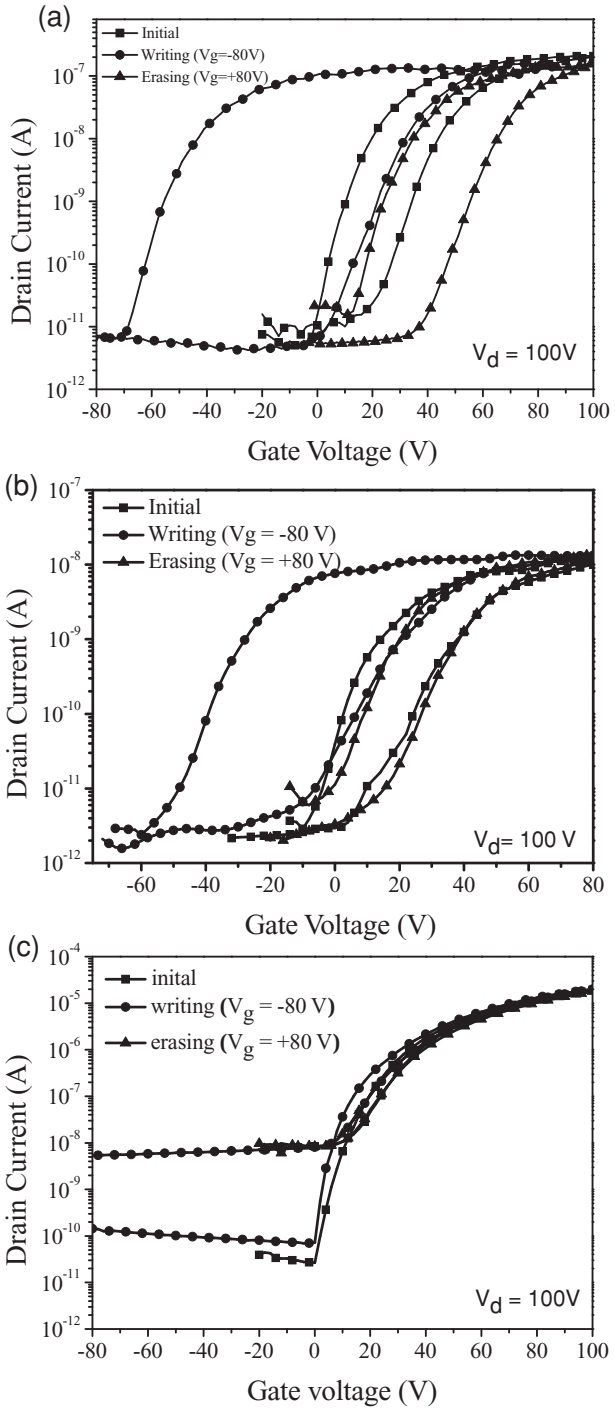

Fig. 5

Figure 5. Transfer characteristics of the BPE-PTCDI: a) NW-P-1, b) NW-B-1, and c) thin film devices (bare substrate), where V_g = –80 and 80 V were applied at V_d = 0 V for the programming and erasing procedures.

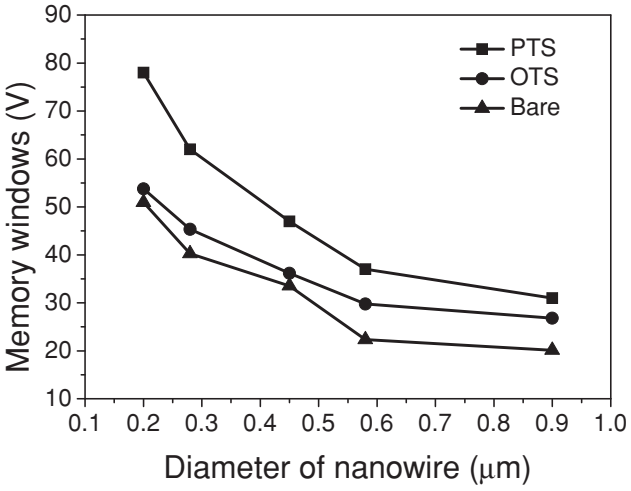

Figure 6. Variation of the memory windows with the nanowire diameter on the BPE-PTCDI OFET memory devices on different SAM-treated substrates.

electrical bistability of the nanowire devices, as summarized in Table 1. The nanowire devices of NW-P-1 and NW-O-1 show the mobilities of 3.4×10^{-2} and 4.3×10^{-3} cm^2 V^{-1} s^{-1}, higher than that on the bare substrates, probably due to the passivation of the silanol groups on the SiO_2 surface through the modification by the SAMs. The enhanced carrier mobilities also increase the ON current, and the passivation on the surface silanol groups efficiently decreases the leakage current. Therefore, the PTS-treated and OTS-treated nanowire devices have the higher on/off current ratios of 2.1×10^4 and 3.8×10^3 at V_g = 0 V, respectively, compared to that of the bare devices (1.4×10^3).

In addition, the SAM modification exhibited a great improvement in the memory windows of the nanowires. **Figure 6** shows the diameters and the memory windows of the BPE-PTCDI nanowire based OFET memory devices on different substrates. The order of the V_{Th} shift at the nanowire devices is PTS-treated substrate > OTS-treated surface > bare surface, which is probably related to the hydrophobicity or π-conjugation on the interface. Baeg et al. reported that the magnitude of the V_{Th} shift was inversely proportional to the degree of hydrophobicity of the dielectric layer.[40] The hydrophilic surface would have a small V_{Th} shift due to the rapid dissipation of transferred charges. The water contact angles for bare, OTS- and PTS-treated surfaces are 47°, 95°, and 78°, respectively (Figure S3 in the Supporting Information). The bare substrate with abundant silanol groups is a highly hydrophilic surface, while the PTS- and OTS-modified substrates are relatively hydrophobic. Therefore, the device on the SAM-treated surface shows the larger V_{Th} shifting than that on the bare surface. Among these memory devices, the PTS-treated devices exhibit the largest V_{Th} shift, even though the contact angle is smaller than the OTS-treated surface. The π-interaction between the phenyl groups of PTS with BPE-PTCDI could facilitate charge trapping in the dielectric-semiconductor interface, resulting in a large V_{Th} shift. We recently found that the magnitude on the memory windows of pentacene OFET was proportional to the fluorene conjugated length of polymer electrets.[73] This indicated that the SAMs with conjugated moiety could improve the charge trapping ability. For comparison, we prepared the BPE-PTCDI thin-film devices as the control devices through vapor deposition on a bare substrate. The OFET mobility and threshold voltage of

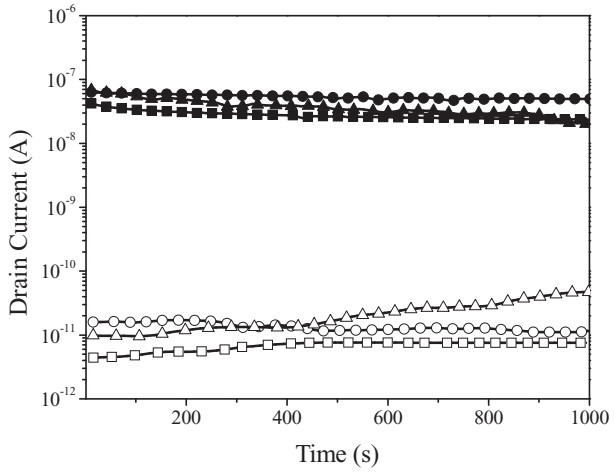

Figure 7. Retention time testing of the OFET memory devices based on BPE-PTCDI nanowires: NW-B-1 (up triangle), NW-O-1 (square) and NW-P-1 (circle). The solid and hollow symbols correspond to the ON and OFF states, respectively.

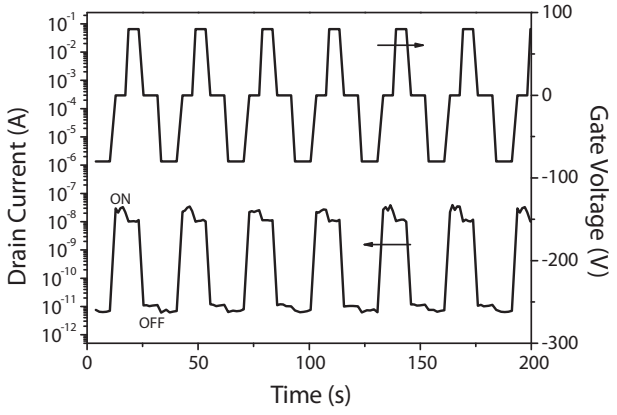

Figure 8. Reversible current response to the WRER cycles of NW-P-1 OFET memory device on the PTS-treated substrate. The drain current was measured at V_d = 100 V. The writing, reading and erasing were at the gate voltages of –80, 0 and 80 V, respectively.

the BPE-PTCDI thin film device are 1.8×10^{-3} cm^2 V^{-1}s^{-1} and 2 V, respectively. The thin film contains abundant gain boundaries (Figure S4 in the Supporting Information) as charge traps, reducing charge transport, and leading to the inferior OFET performance compared to nanowires. These results reveal that the combination of the small BPE-PTCDI nanowires and the hydrophobic substrates can produce the high-performance of OFET-type memory devices. On the other hand, the V_{Th} shifts are inversely proportional to the diameter of nanowires for all three kinds of substrates because they can induce a higher electric field. The combination of the high electrical field and the conjugated functional groups could be an effective approach to stabilize the metastable trapping states at the interface between the nanowires and the dielectric layer.

The time during which the stored charge is retained in the dielectric layer is defined as the retention time. **Figure 7** is the retention time of the BPE-PTCDI nanowires on bare, OTS-treated and PTS-treated substrates. The retention time of the ON and OFF states of the device at a gate voltage of 0 V are maintained for 10^3 s with a high on/off current ratio of around 10^3–10^4. The PTS-treated device shows superior stability and longer retention time for at least 10^4 s, probably due to the hydrophobic surface, reducing the release of trapped charges. On the other hand, the on/off ratio of the bare device exhibited a fast decay, attributed to the hydrophilic surface. The above results revealed the significance of the dimension and surface modification on the characteristics of the semiconducting nanowire OFET memory devices, such as the mobilities, on/off current ratio (V_g = 0 V) and memory windows. The multiple switching stability of the nanowire NW-P-1 device was evaluated through write-read-erase-read (WRER) cycles, as shown in **Figure 8**. The operation conditions of WRER cycles are summarized as the following. The drain current was measured at V_d = 100 V. The writing, reading and erasing processes were at the gate voltages of –80, 0 and 80 V, respectively. An ON/OFF current ratio of more than 10^3 was achieved in WRER cycles. The responding ON and OFF currents of the device could be maintained over 100 cycles (Figure S6 in the Supporting Information). The good stability and reversibility suggested the potential applications using organic semiconducting nanowires for nonvolatile flash-type memories.

To investigate air stability, the electrical performance of nanowire device was characterized in ambient atmosphere and compared to that in inert atmosphere, as shown in **Figure 9**. Relative humidity ranges from 50 to 60% in air. Under the ambient atmosphere, the field-effect mobility and memory window of the NW-P-1 device were 3.2×10^{-2} cm^2 V^{-1} s^{-1} and 73 V, respectively, similar to the performance measured in insert atmosphere. It indicates residual water and oxygen did not have a significant effect on both charge transport and memory behaviors. On the other hand, under ambient atmosphere, the retention time of ON and OFF states could be maintained for 10^4 s, and the on/off current ratios are 10^3–10^4 without significant degradation. This suggested that this n-type organic semiconducting nanowire device possessed superior air stability under ambient conditions, beneficial to practical applications of nonvolatile memory devices.

3. Conclusions

We have demonstrated nonvolatile OFET memory devices using organic n-channel BPE-PTCDI nanowires. The diameters and crystallinity of the nanowires were manipulated through controlling the non-solvent composition and significantly affected the charge transport and memory behaviors, such as the mobilities, on/off current ratio (V_g = 0 V) and memory windows. The memory windows was enhanced with decreasing the nanowire diameter, presumably due to the high electrical field induced from the confined dimension. The memory window was further enhanced using the hydrophobic surface by self-assembled monolayer. Besides, the nanowire device exhibited good air stability, indicating that residual water and oxygen did not have a significant effect on the bistable switching. Our study revealed the potential applications of organic n-type semiconducting nanowires for nonvolatile OFET memory devices.

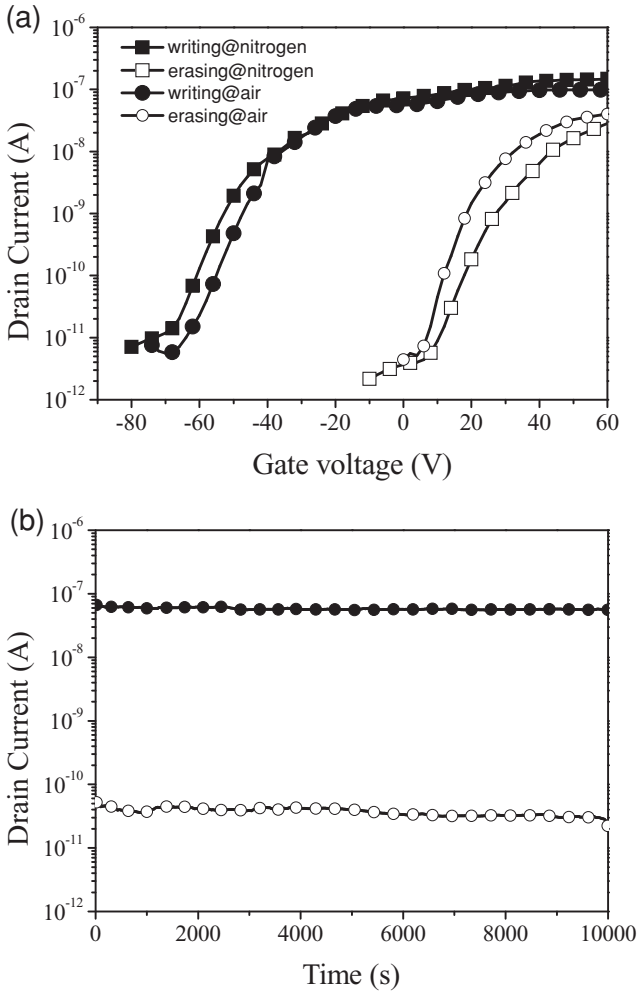

Figure 9. a) Transfer curves of the NW-P-1 device in N_2-filled atmosphere and ambient conditions, where V_g = –80 and 80 V were applied at V_d = 0 V for the writing and erasing procedures. b) Retention time testing of the NW-P-1 device in air. The solid and hollow symbols correspond to the ON and OFF states, respectively.

4. Experimental Section

Preparation of the BPE-PTCDI Nanowires: BPE-PTCDI was purchased from Luminescence Technology Corp (Taiwan). To induce the nanowire structure, BPE-PTCDI was dissolved in refluxing *o*-dichlorobenzene in a round-bottom flask with magnetic stirring and heated to 160 °C. After the powder was completely dissolved in solution at the high temperature of 160 °C, methanol as a non-solvent was slowly added into the organic solution to induce crystallization. As the solution cooled, its color changed gradually from orange to dark green. After several hours, cotton-like BPE-PTCDI nanowires were observed floating in the solution. The compositions of the methanol non-solvent, 20, 40, 60, 75, and 90 vol%, in *o*-dichlorobenzene were used to prepare the BPE-PTCDI nanowires with different diameters and lengths.

Characterization: UV–vis absorption spectrum was recorded on a Hitachi U-4100 spectrophotometer. For the thin film spectra, BPE-PTCDI was vapor-deposited onto quartz substrate at 90 °C. On the other hand, BPE-PTCDI nanowire in mixed solvent was drop-coated onto quartz substrate for the nanowires spectra. The absorption spectra of the BPE-PTCDI solution in *o*-dichlorobenzene were also recorded. The morphology of the nanowires was determined using a field emission scanning electron microscope (SEM, JEOL JSM-6330F). The FE-SEM images were taken using a microscope operated at an accelerating voltage of 10 kV. Before imaging, the samples were sputtered with Pt. X-ray diffraction (XRD) was performed by X'Pert PRO X-ray diffractometer using Cu-Kα radiation (λ = 1.5418 Å) with a scan range typically of 5–30°, 0.2° per step.

Device Fabrication and Characterization: The transistor-type memory devices based on BPE-PTCDI nanowires were fabricated on a wafer with a thermally grown 300-nm thick SiO_2 dielectric on highly doped n-type Si as a gate electrode. Trichloro(phenyl)silane (PTS) and trichloro(octyl)-silane (OTS) were obtained from Aldrich Chemical Co. PTS- or OTS-treated surface on SiO_2 were prepared by the following procedures: the cleaned substrates were immersed into a 10 mM solution of PTS or OTS in anhydrous toluene at room temperature for 2 hours. Then, the substrates were rinsed with toluene, acetone, isopropyl alcohol, and dried with a steam of nitrogen. Then, nanowires in solution were spin-coated at 1000 rpm for 60 s onto PTS-, OTS-treated or bare substrates. The nanowires were dried under vacuum (10^{-6} Torr) at 70 °C for overnight to remove residue solvents. The thin film of BPE-PTCDI was prepared by thermally deposition with a deposition rate of 0.3–0.4 nm s^{-1} at 90 °C under vacuum (10^{-7} Torr) to form a 50-nm-thick film. The top-contact source and drain electrodes were defined by 80 nm-thick gold through a regular shadow mask, and the channel length (L) and width (W) were 50 and 1000 μm, respectively. The current–voltage (I–V) characteristics of the devices were measured by using a Keithley 4200-SCS semiconductor parameter analyzer in a N_2-filled glove box or in air.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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